**Digital Design and Computer Organization Laboratory**

**UE19CS206**

**3rd Semester, Academic Year 2020-21**

Date:7/9/2020

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| Name:  SUMUKH RAJU BHAT | SRN:  PES1UG19CS519 | Section:  H |

Experiment Number: 2 Week# 3

Program Number : 1

**Title of the Program: Ripple Carry Adder**

// Module 4-bit ripple carry adder.

module fulladdR(input wire [3:0] a, b, input wire cin, output wire [3:0] sum, output wire cout);

// Instantiate full adder modules here.

wire [2:0] c;

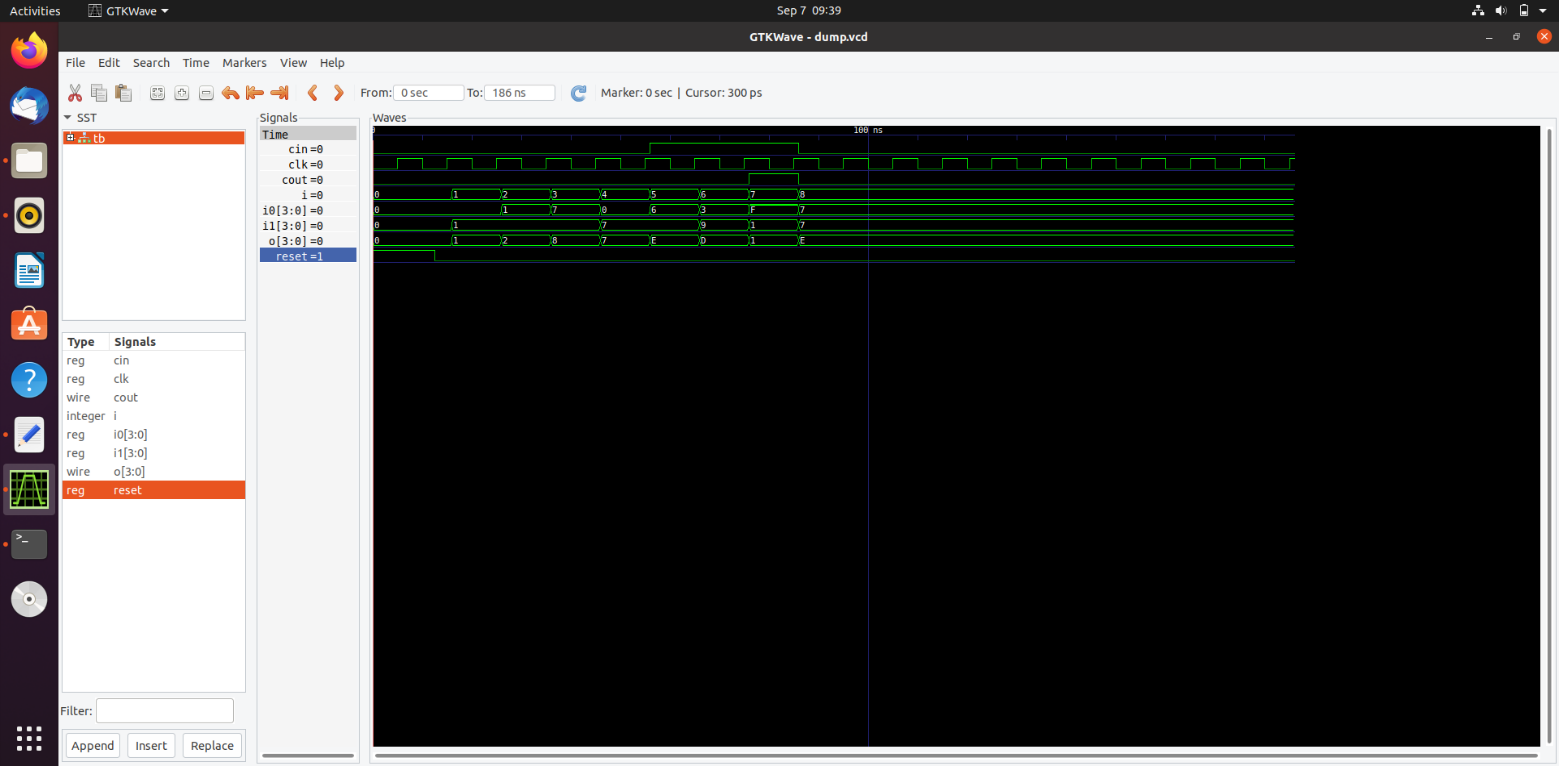
fulladd f0(a[0],b[0],cin,sum[0],c[0]);

fulladd f1(a[1],b[1],c[0],sum[1],c[1]);

fulladd f2(a[2],b[2],c[1],sum[2],c[2]);

fulladd f3(a[3],b[3],c[2],sum[3],cout);

endmodule

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Program Number : 2

**Title of the Program: 4 to 1 MUX**

module mux4 (input wire [0:3] i, input wire j1, j0, output wire o);

wire t0, t1;

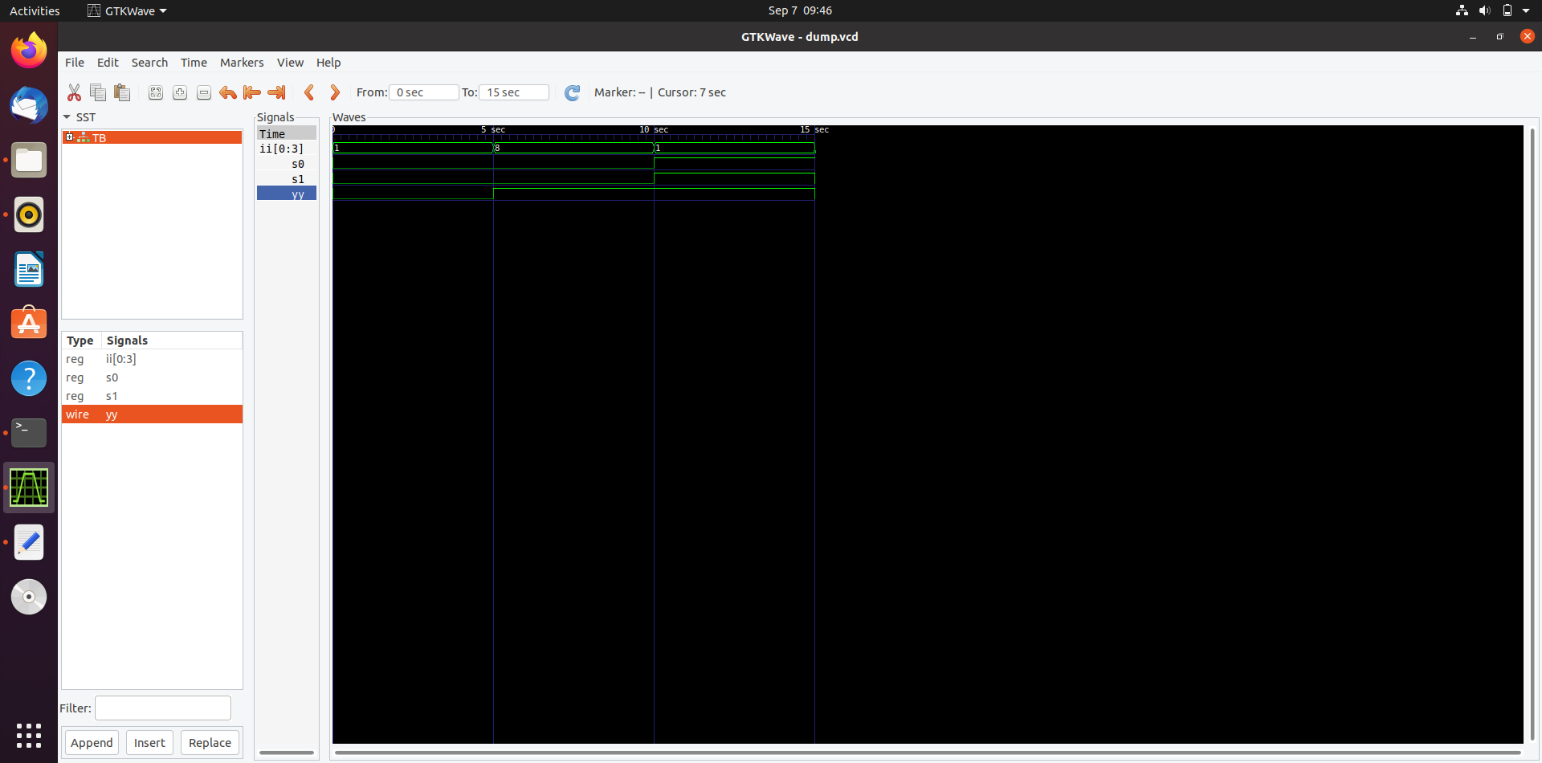
//Write your code here (Use only 2:1 Mux)

mux2 m1(i[0],i[1],j0,t0);

mux2 m2(i[2],i[3],j0,t1);

mux2 m3(t0,t1,j1,o);

endmodule

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